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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,463	03/30/2000	Charles W. Selvidge	M-8288 US	8093

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	12

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/539,463	SELVIDGE ET AL.
	Examiner	Art Unit
	Dwin M Craig	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4-8-2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been presented for reconsideration based on Applicant's arguments.

Response to Arguments

2. Applicants arguments submitted on 4-8-2004 have been fully considered. The Examiner's response is as follows.

2.1 Regarding Applicant's response to the Examiner's objections to the drawings because of a missing reference to an emulation system, item 100:

Applicant argued:

> The drawings are objected to for not including a reference to the emulation system 100 as disclosed in the specification. Applicants request that Figure 1 be amended as shown in the attached Appendix. Applicants believe that such an amendment renders the objection moot.

The Examiner has reviewed the file wrapper and cannot locate ~~and attached~~ any attachment labeled Appendix as suggested by the Applicant. The Examiner respectfully requests that Applicant provide another copy of said appendix in response to this Office Action.

2.2 Regarding Applicant's response to the 35 U.S.C. 103 rejections of Claims 8-14 and 14-16:

Applicant argued:

> Applicants respectfully submit that 35 U.S.C. 103(c) prevents Marantz from being relied upon in a 35 U.S.C. 103(a) rejection. A1: the time the present application was filed (and thus at the time the present invention was made by constructive reduction to practice), Marantz was owned by Ikos. Also, at the time the present application was filed, the inventors of the present application were obligated to assign the present application to Ikos. Because Marantz and the claimed invention were, at the time the invention was made, owned or obligated to be owned by the same entity, 35 U.S.C. 103(c) prevents Marantz from being used to reject the present invention under 35

U.S.C. 103(a). Therefore, Applicants respectfully request that the rejection of claims 8-10 and 14-16 be withdrawn.

Applicant's arguments have been persuasive and the Examiner withdraws the 35 U.S.C. 103(a) rejections of Claims 8-10 and 14-16.

2.3 Regarding Applicants response to the 35 U.S.C. 103(a) rejection of Independent Claim 1:

Applicant argued:

Not surprisingly, the background section of Barr describes a system that is different from Barr's own system. Therefore, the rejection of claim 1 actually attempts to combine three different systems: (1) Sample; (2) the *invention of* Barr (alleged to disclose a framing sequence); and (3) the *prior art* to Barr (alleged to disclose serial packet transmission and that each bit is transmitted over two transmit clock periods). Applicants respectfully submit that the rejection does not make out a *prima facie* case of obviousness, because the Office Action does not suggest that a motivation existed to combine the prior art system of Barr with Barr's own system.

The Examiner respectfully asserts that, as per the requirement in the in *Graham* **v.** *John Deere* case wherein the Examiner must consider objective evidence present in the application indicating obviousness or nonobviousness, the *Sample et al.* reference clearly discloses that one of the possible embodiments of the invention disclosed, is **Col. 11 Lines 25-29** *"Encoding schemes using pulse-width modulation, phase shift modulation and serial encoding can reduce power consumption and increase the relatively low operating speed intrinsic to the simplest form of time-multiplexing."* The Examiner respectfully asserts that the *Sample et al.* reference clearly discloses that there is a need in the art for *serial encoding* when it comes to multiplexing different signals between FPGA's for the purpose of emulation. This motivation would lead an artisan of ordinary skill to look for methods of performing *serial encoding* and thus lead to the combination of the *Barr* reference and the *Sample et al.* reference.

Applicant has also argued...

> Indeed, one of ordinary skill in the art would actually have been *discouraged* from combining the prior art system disclosed in Barr with the invention of Barr. Barr disparages, and teaches away from, using two or more transmit clock periods for each bit in Barr's own invention. Barr observes that the prior art system disclosed in the background of Barr requires too many clock periods and therefore uses excessive bandwidth. Sec, e.g., Barr, col. 3, Ins. 1-4 and 59-61. The invention of Barr seeks to reduce this bandwidth. Id.
>
> Applicants also note that the Office Action relies upon Barr's background discussion of pilot tones (col. 1, In. 33) to disclose the claimed framing sequence. However, Barr does not teach or suggest that the pilot tone is a framing sequence that is transmitted serially over a connection between asynchronous systems in accordance with a transmit clock signal, as required by claim 1. Nor does Barr even teach or suggest that the pilot tone has bits, as does the claimed framing sequence in claim 1. Nor does Barr teach or suggest that the pilot tone has bits that are transmitted over two transmit clock periods, as claim 1 requires of the recited framing sequence.

The Examiner asserts that, *by Applicant's own Admission,* using two clock periods is not the *best mode* with which to enable Applicant's claims. The Examiner maintains that an artisan of ordinary skill would have been motivated to look in the high-speed digital communications art by the teachings in the *Sample et al.* reference. The Examiner asserts that any digital communications over a serial interface has to be framed whether that interface is an RS-232, T1, T3, E1, E3, ATM or any other serial interface, the information has to be framed in order to be sent from the transmitter to the receiver. The Examiner asserts that the *Barr et al.* reference teaches that the method of using two transmit clocks, as claimed by Applicant, is known in the art, **(*Barr et al.* Col. 2 Lines 40-47).** The Examiner has found Applicants arguments to be unpersuasive and upholds the 35 U.S.C. 103(a) rejection of Independent Claim 1.

2.4 As regards Applicant's arguments concerning Independent Claim 2:

See paragraph 2.3 above.

2.5 As regards Applicant's arguments concerning Independent Claims 5 and 11:

Applicants argued:

> The Office Action alleges that it would have been desirable to combine these teachings in order to synchronize over a wide range of sampling rates, citing col. 3, his. 29-34 of Barr. However, such a desire expressed in Barr is supposedly solved, not by the background system disclosed in Barr, *but by the invention of Barr itself. In* other words, the motivation cited by the Office Action is entirely unrelated to the background system disclosed in Barr that is proposed to be combined with Sample. Applicants therefore respectfully submit that a valid motivation to combine Sample with the *background system* disclosed in Barr itself has not been provided, and that a *prima* facie case of obviousness has not been made.

The Examiner asserts, as argued above, the *Sample et al.* reference points to the *digital serial communications art,* as disclosed in *Barr et al.* and that *by Applicant's Own Admission* the *Barr et al.* reference teaches the claimed limitations. The Examiner asserts that the prior art teaches the claimed limitations and that the combination is proper for at least the reasons given in these response to arguments *(see section 2.3 above).* The Examiner has found Applicant's arguments to be unpersuasive and upholds the 35 U.S.C. 103(a) rejections of Claims 1, 2, 5, 11, 3, 4, 6, 7, 12 and 13.

An updated search has revealed new art.

Drawings

3. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed. The drawings filed on 3/30/2003 are acceptable subject to correction of the formalities listed in the attached "Notice of Draft person's Patent Drawing Review," PTO-948.

3.1 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: *"emulation*

system 100" as disclosed in lines 1-2 on page 5 of the specification does not appear in Figure 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1-16** are rejected under 35 U.S.C. 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed. Evidence of concealment of the best mode is based upon, *Applicants Own Admission (see section 2.3 above and paper number11 page 6)* where the use of two transmit clocks per data bit uses up to much bandwidth, *Barr et al. Col. 3 Lines 1-4.* The current claim language is therefore not claiming the best mode for operating Applicant's emulation system.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181.**

5.1 As regards independent **Claims 1 and 2** the *Sample et al.* reference discloses a logic emulation system **(Figure 1, Col. 6 Lines 39-57 & Figure 12),** providing a transmit clock signal of a predetermined clock frequency **(Figure 10 Item 144, Col. 19 Lines 15-29 and Figure 19 Item 200),** a method for transmitting a data packet between substantially asynchronous components **(Figure 10, Col. 13 Lines 43-62, Col. 14 Lines 6-10),** transmitting serially over a connection between asynchronous systems **(Col. 10 Lines 39-47, Col. 10 Lines 66-67, Col. 11 Lines 1-21)** and a framing sequence **(Col. 24 Lines 67, Col. 25 Lines 1-19).**

However the *Sample et al.* reference does not expressly disclose a framing sequence, subsequent to transmitting the framing sequence transmitting a data packet serially, and each bit of the framing sequence is transmitted over two transmit clock periods.

The *Sample et al.* reference discloses that, the use of serial data encoding techniques can reduce power consumption and increase the speed *(performance)* of the emulation system **(Col. 11 Lines 22-36).** An artisan of an ordinary level of skill would have looked in the high speed interface protocol art to find a method to send data over a asynchronous serial link and preserve

the clock information in order to lower the power consumption of the emulator and reduce the power consumption. In the digital communications art the *Barr et al.* reference discloses a framing sequence **(Figure 1 & Col. 1 Lines 30-37 & Col. 3 Lines 62-68),** subsequent to transmitting the framing sequence transmitting a data packet serially **(Col. 4 Lines 18-31),** and each bit of the framing sequence is transmitted over two transmit clock periods **(Figure 2(B) & Col. 2 Lines 40-47).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the emulation technology of the *Sample et al.* reference with the asynchronous digital communications technology of the *Barr et al.* reference because it is desirable to be able to synchronize over a wide range of sampling rates **(Barr et al. Col. 3 Lines 29-34).**

5.2 As regards independent **Claims 5 & 11** *see paragraph 3.1 above.* Further, as regards the limitation of having a plurality of programmable logic devices the *Sample et al.* reference discloses **(Col. 1 Lines 10-23),** and a controller coupled to a host computer **(Figure 14 Item 540).**

5.3 As regards dependent **Claim 3** the *Sample et al.* reference discloses different circuit boards in a chassis **(Figure 13).**

5.4 As regards dependent **Claims 4** the *Sample et al.* reference discloses a controller housed in a host computer **(Figure 19 Item 500).**

5.5 As regards dependent **Claims 6, 7, 12 & 13** the *Sample et al.* reference discloses a master clock signal being generated on a separate controller board **(Figure 19).**

6. **Claims 8-10 and 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample et al. U.S. Patent 5,690,191** in view of **Barr et al. 5,297,181** and in further view of **Selvidge et al. U.S. Patent 5,659,716.**

6.1 As regards independent **Claims 5 and 11** see paragraphs **5.1** and **5.2** above.

6.2 As regards dependent **Claims 8-10** and **14-16** the *Sample et al.* reference does not expressly disclose *"virtual clocks"*.

The *Selvidge et al.* reference discloses *Virtual Clocks* **(Col. 5 Lines 63-67, Col. 6 Lines 1-7).**

It would have been obvious, to one of ordinary skill in the art, at the time the inventions was made, to have combined the emulation technology of the *Sample et al.* reference with the *Virtual Clock"* technology of the *Selvidge et al.* reference because the *Virtual Clock* technology coupled with the de-multiplexing methods and technology of the *Selvidge et al.* teachings provides a method of performing emulation with fewer pin count, **(Selvidge et al. Col. 2 Lines 5-15).**

Conclusion

7. **Claims 1-16** have been rejected. This action is **NON-FINAL.**

7.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC